Lab 0 info

Combinational gates example was simulated successfully to our TA - source code not included in this folder since it is the same as the CCLE files

TB file - file has not been modified from the initial simulation activity - our computer would not let us simulate at first, so we got approval from our TA, Logan Kuo to skip the simulation portions and go straight to the board

UCF file - see uncommented portions taken from the Nexys file in the src folder on CCLE

.v file - has code for the clock divider

**\*\*\*\*\*\*\*\*\*STILL NEED SOURCE CODE FOR FOUR BIT COUNTER AND MODERN VERSION**